In the Specification:

Please replace the paragraph beginning at page 2, line 15, with the following rewritten paragraph:

--It is another object of the present invention to provide improved structure of FCBGA and manufacture thereof. The redistribution and solder-bump process for a conventional structure of FCBGA are simplified and integrated into the fan-out process of build-up substrate.--

Please replace the paragraph beginning at page 2, line 26, with the following rewritten paragraph:

-- In the present invention, a semiconductor packaging device has a carrier having at least a cavity or a slot thereon for fitting at least a chip. The chip has a back surface, an active surface with a plurality of first bonding pads, and a sidewall connecting the back surface and the active surface. The back surface and the sidewall of the chip are affixed to the cavity and expose the active surface. A first insulating layer is coated on both the active surface and the carrier, and has first conductive holes therein. The first conductive holes are corresponding to first bonding pads. A multi-layer structure is on the first insulating layer, which has conductive layout lines, second conductive holes therein, a second insulating layer thereon and exposed ball pads in the second insulating layer. The first conductive holes are electrically connected with the conductive layout lines, the second conductive holes, and the exposed ball pads. A plurality of solder balls are affixed to the ball pads. Such architecture integrates the redistribution and fan-out process, which simplifies the conventional process for flip-chip ball grid array.--

Please replace the paragraph beginning at page 5, line 8, with the following rewritten paragraph:

-- In the present invention, a semiconductor packaging device has a carrier having at least a cavity or a slot thereon for fitting at least a chip. The chip has a back surface, an active surface with a plurality of first bonding pads, and a sidewall connecting the back surface and the active surface. The back surface and the sidewall of the chip are affixed to the cavity and expose the active surface. A first insulating layer is coated on both the active surface and the carrier, and has first conductive holes therein. The first conductive holes are corresponding to first bonding pads. A multi-layer structure is on the first insulating layer, which has conductive layout lines, second conductive holes therein, a second insulating layer

thereon and exposed ball pads in the second insulating layer. The first conductive holes are electrically connected with the conductive layout lines, the second conductive holes, and the exposed ball pads. A plurality of solder balls are affixed to the ball pads. Such architecture integrates the redistribution and fan-out process, which simplifies the conventional process for flip-chip ball grid array.--

Please replace the paragraph beginning at page 7, line 22, with the following rewritten paragraph:

--FIGS. 3-5 are cross-sectional views illustrating the packaging chip cut with line 2A-2A of FIG. 2. Depicted in FIG. 3, solder balls are distributed on the surrounding of the chip. After the chip 20 is placed in the carrier 11 and affixed by an adhesive 19, an insulating layer 14 is formed on the active surface 30 of the chip 20 and the carrier 11 where the bonding pads 21 of the chip 20 are exposed. Multitudes of plating through 22 in the insulating layer 14 are corresponding and electrically connected to the bonding pads 21. A multi-layer film 15 with predetermined circuit 23 and plating through holes 40 is on the insulating layer 14 and thereafter another insulating layer 16 is formed on the multi-layer film 15 only to expose the pads 18 of the plating through holes 40 on which the solder balls 17 are affixed, and the solder balls are distributed on the carrier 11, the chip 20, or both. Thus, the pad redistribution, bumping, and fan-out processes for the chips can be implemented at same process. One of advantages of the present invention is to avoid the direct chip attachment to a print circuit board for fear of poor reliability. Furthermore, the packaging thickness is minimum and the heat radiation is improved.—

In the Claims:

Claim 1 (currently amended): A semiconductor packaging device comprising:

a carrier having at least a cavity thereon, said cavity configured for fitting a chip;

said chip having a back surface an active surface, and a sidewall connecting said back surface and said active surface , wherein said back surface and said sidewall are affixed to said cavity and exposed said active surface, and said active surface has a plurality of first bonding pads;

a first insulating layer coated on said active surface and said carrier and having a plurality of first conductive holes therein, wherein said first conductive holes correspond to first bonding pads;

a multi-layer structure on said first insulating layer, said multi-layer structure having a plurality of conductive layout lines, a plurality of second conductive holes therein, a second insulating layer thereon, and a plurality of exposed ball pads in said second insulating layer, wherein said first conductive holes are electrically connected with said conductive layout lines, said second conductive holes, and said exposed ball pads; and

a plurality of solder balls affixed to said exposed ball pads.

Claim 2 (currently amended): The semiconductor packaging device of claim 1, wherein said carrier is made of a material selected from groups consisting of a silicon substrate, a ceramic substrate, a glass substrate, an organic substrate, or combination of above.

Claim 4 (currently amended): The semiconductor packaging device of claim 1, wherein said ball pads are distributed at a location selected from the groups consisting of above said chip, above surrounding of said chip, and both above said chip and above surrounding of said chip.

Claim 13(New): A semiconductor packaging device comprising:

a carrier having at least a cavity thereon, said cavity configured for fitting a chip;

said chip having a back surface, an active surface, and a sidewall connecting said back surface and said active surface, wherein said active surface has a plurality of first bonding pads;

an adhesive affixing said back surface and said sidewall to said cavity;

a first insulating layer coated on said active surface and said carrier and having a plurality of first conductive holes therein, wherein said first conductive holes correspond to first bonding pads;

a multi-layer structure on said first insulating layer, said multi-layer structure having a plurality of conductive layout lines, a plurality of second conductive holes therein, a second insulating layer thereon, and a plurality of exposed ball pads in said second insulating layer, wherein said first conductive

holes are electrically connected with said conductive layout lines, said second conductive holes, and said exposed ball pads; and

a plurality of solder balls affixed to said exposed ball pads.

In the Drawings:

The attached sheet of drawings includes changes to FIGS. 3 through 7.

Attachment: Replacement Sheet